

**PATENT**  
**IBM Docket No. RAL999-0080**

**Amendments to the Claims:**

**1 - 9. (Canceled)**

**10. (Currently amended) A method comprising the steps of:**  
**storing in an a single instruction memory instructions for the handling of**  
**data transiting an interface device;**  
**executing in a plurality of interface processors the instructions stored in**  
**the single instruction memory;**  
**receiving a data flow inbound through an input port;**  
**communicating the data flow through the plurality of interface**  
**processors; and**  
**directing the data flow outbound through an output port in accordance**  
**with the execution of the instructions by the interface processors.**

**11. (Original) A method according to Claim 10 further comprising parsing**  
**the data flow into a plurality of portions, storing selected portions of the**  
**parsed data flow in data memory, and directing other selected portions of the**  
**parsed data flow to a switching fabric for determination of an outbound**  
**direction.**

**12. (Original) A method according to Claim 11 further comprising**  
**recombining the stored and other selected portions of the data flow prior to**  
**direction of the data flow outbound through an output port.**

**13. (Original) A method according to Claim 10 wherein the step of**  
**communicating the data flow through the plurality of interface processors**

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**comprises parsing the data flow into portions and distributing the parsed portions among the plurality of interface processors for handling in parallel.**

**14 - 42 (Canceled)**

**43. (New) A method according to claim 10 further comprising storing in a control processor control information including initialization and configuration data; and**

**forwarding stored information to selected ones of said plurality of interface processors.**

**44. (New) The method according to claim 43 wherein the control information is forwarded in a packet formatted with a protocol compatible for a network coupling the control processor and the interface processors.**